REMARKS

Claims 13-24 and 26 are pending. Claims 13 has been amended to incorporate the features of claim 25.

Claims 13, 15, 17 and 21 were rejected under 35 USC §102(e) as being anticipated by Shimawaki. This rejection has been rendered moot by the present amendment of claim 13 incorporating the features of claim 25.

Claim 20 was rejected under 35 USC §103(a) as being unpatentable over Shimawaki in view of Hashimoto et al. It is believed that this rejection has also been rendered moot.

Claim 13 has been amended to clarify that the present invention relates to InP/GaInAsSb based HBT. InP and GaInAsSb have different etching characteristics. Thus, the selective etching can be used in etching the InP emitter layer on the GaInAsSb base layer (corresponding to the step of patterning the second semiconductor layer). According to this feature of the present invention, the base layer beneath the second semiconductor layer can be easily exposed in order to form the base contact layer thereon. Thus, according to the present invention, the increase of the fabrication yield is expected.

On the other hand, Shimawaki relates to A1GaAs/GaAs based HBT. The graded layer is formed between the base layer and the emitter layer, and between the base layer and the collector layer. Thus, the above-described specific effect of the present invention cannot be achieved by Shimawaki.

Hashimoto et al. teaches thermal treatment for eliminating hydrogen. However, the thermal treatment of Hashimoto et al. is conducted in order to eliminate hydrogen termination and/or OH group terminations adhered to the surface of the base layer. The thermal treatment of Hashimoto et al. is to modify surface state of the base layer. On the other hand, in the present invention, the thermal treatment is conducted in order to eliminate hydrogen in the base layer introduced into the base layer during the deposition of the base layer by MOCVD. The thermal treatment of the present invention is to improve the film quality of the base layer. Thus, the thermal treatment of Hashimoto et al. is clearly different from the present invention.

As described above, Shimawaki and Hashimoto et al. are clearly different from the present invention. Thus, the present invention would not have been obvious to one of ordinary skill in the art, even if Hasimoto et al. is further considered.

Claim 25 was rejected under 35 USC §103(a) as being unpatentable over Shimawaki and further in view of Frank et al. Favorable reconsideration of this rejection is earnestly solicited.

The Examiner states that Frank et al. discloses an emitter layer of an InP layer, so that it would have been obvious to one of ordinary skill in the art at the time of the present invention to use the InP emitter layer of Frank et al. as the second semiconductor layer in the method of Shimawaki in order to improve transistor characteristic by increasing the electron mobility when compared with an AlGaAs emitter layer as taught by Frank et al. in column 5, lines 51-63.

However, Frank et al. relates to InP/GaAsSb based HBT, so that the HBT of Frank et al. is basically different from the AlGaAs/GaAs based HBT of Shimawaki. The selection of the

composition materials depends on the base structure of HBT. If the base structures differ from each other, selections of materials also differ from each other. Thus, the teachings of Frank et al. fail to provide any motivation to modify Shimawaki in a manner suggested by the Examiner.

Additionally, one of ordinary skill in the art would not apply the InP to the emitter layer of Shimawaki's HBT. In Shimawaki, the base layer is formed of $In_xGa_{1-x}As$ (x: 0.1 ~ 0), so that when the InP emitter layer is formed on the base layer, the emitter layer is completely strained because of the lattice mismatch therebetween and no merits are obtained by the use of InP emitter. In the present invention, an InP emitter layer is used in order to lattice-match the emitter layer with the base layer.

For at least the foregoing reasons, the claimed invention distinguishes over the cited art and defines patentable subject matter. Favorable reconsideration is earnestly solicited.

Should the Examiner deem that any further action by applicants would be desirable to place the application in condition for allowance, the Examiner is encouraged to telephone applicants' undersigned attorney.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 50-2866.

Respectfully submitted,

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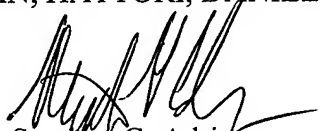

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